Review
総　説

Novel Technology for Digital Controlled UPS Inverter

Lipei Huang* Yadong Liu** Meng Wang***

*Dept. of Electrical Engineering, Tsinghua University, Beijing 100084, China
**Philips Research Asia-Shanghai, Lane 888, Tianlin Road, Shanghai 200233, China
***School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853, U.S.A

Abstract

A novel digital PID control scheme for UPS inverter based on digital signal processing (DSP) is proposed in this paper. The capacitor current of output filter comes from the differential of the measurement of output voltage. Thus, a quasi double loop control is achieved. The analysis on dead time effect allows us to propose its compensation method to weaken the effect and reduce the total harmonic distortion (THD) in the output voltage in steady state. Experimental results show that the quasi double loop control with dead time compensation is effective. Moreover, to limit the output voltage distortion and improve the performance of UPS inverters, a novel robust deadbeat control method is proposed in this paper to deal with the problem. In this control method, a proportional element is added to the traditional deadbeat control in order to improve the robustness to parametric imprecision. Experimental results show that the robustness for parametric variation of the proposed method is much better than the traditional deadbeat control. This method has also very good static performance under linear load or nonlinear load compared with digital PID control. Therefore, this novel technology is easy to be realized in DSP and suitable for full digital realization of UPS.

Key words: UPS inverter; Deadbeat control; Robustness

1 Introduction

UPS has been widely used in the fields of communication, networks, medical treatment, etc, feeding various critical loads such as communication device, computer server, and life support system. Low total harmonic distortion (THD) in the output voltage of UPS inverter under various loads and fast dynamic response in presence of unknown distorting load are the main requirement for high-performance UPS.[1] It is worth noting that maintaining low distortion waveform under rectifier load is especially important in order to ensure that the usual loads, computers, and communication devices work well.

Conventionally, the controllers of UPS inverter were usually designed by frequency-domain-based analog control scheme. Compared with the analog implementation, digital control based on microprocessor has many advantages such as no aging effect, avoiding temperature drift, and easy adjustment of control parameters.[2]

In this paper, a novel digital control scheme was proposed. It has two features: (1) neither the output-filtering capacitor current nor inductor current is sensed; instead, the capacitor current needed by internal loop is from the differential of the output voltage and (2) a dead time compensation method is proposed to improve the performance in steady state.

To limit the output voltage distortion and improve the performance of UPS inverters, various digital control methods have been proposed[2-4], such as repetitive control, deadbeat control, and sliding mode control.

Deadbeat control, which originated from state equations, has very fast dynamic response and can eliminate voltage variation in several control periods.[4] However, stability of deadbeat control is poor especially when the inverter feeds no load; robustness is poor, that is, the control performance is sensitive to parameters of output filter. A robust deadbeat control method is proposed to solve this problem. This method adds a proportional element to the traditional deadbeat control and can effectively improve the robustness of deadbeat control with the expense of little increased static error and slower dynamic response.

2 Structure of digital controlled UPS inverter

An UPS inverter is usually a voltage source SPWM inverter in series with output filter. Take the half bridge inverter with IGBT switches as example, as shown in Fig. 1. The output filter consists of an inductor and a capacitor with equivalent series resistance (ESR) r_L and r_C, respectively. In approximate analysis, the two ESR can be assumed to be zero.

The inverter is a nonlinear system due to the existence of power switches. Fortunately, the SPWM modulation stage can be considered as an approximate proportional element, since the switching frequency is much higher than the bandwidth of control system, and most of high frequency component will be absorbed by output filter. Then the modeling of main circuit part of inverter can be shown as Fig. 2. u_x is the calculation result of digital signal processing (DSP) controller acting as reference wave in PWM modulation stage. $<u_{in}>$ is the average value of u_{in} in a control period (half of switching period in this paper).

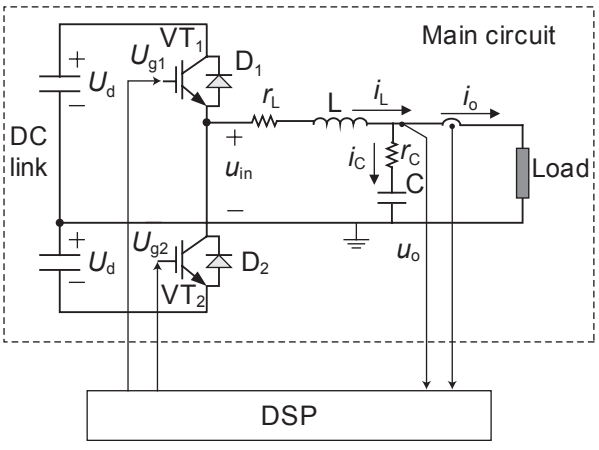

Fig. 1　Equivalent circuit of a half bridge UPS inverter.

3 Digital control scheme

3.1 Quasi double control

Multi-loop control has been researched in some papers.[2] In these control schemes, in addition to output voltage feedback loop, output filtering capacitor current or inductor current is also sensed to constitute a faster internal feedback loop. This sensing is conducive to widen the bandwidth of control system and improve the dynamic response of inverter.

According to Fig. 1, it holds:

$$i_c = C\frac{du_o}{dt} \tag{1}$$

Equation 1 shows that the capacitor current can be got by differentiating the output voltage. Noting that differential element can be easily got using backward Euler method or Trapezoidal Rule in DSP, the current sensor for capacitor current can be saved. Then quasi double loop control can be got as shown in Fig. 3.

$G_v(s)$, $G_i(s)$, and $G_h(s)$ are voltage controller, current controller, and zero order hold element, respectively.

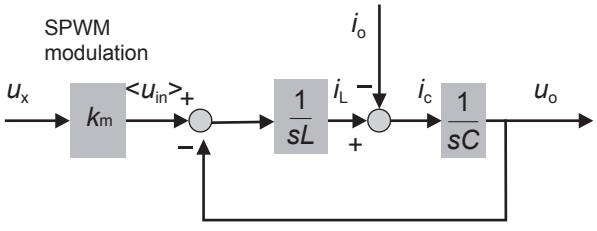

Fig. 2　Modeling of main circuit of UPS inverter.

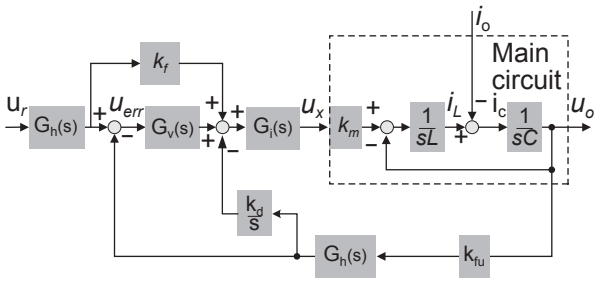

Fig. 3 Block diagram of quasi double loop control system.

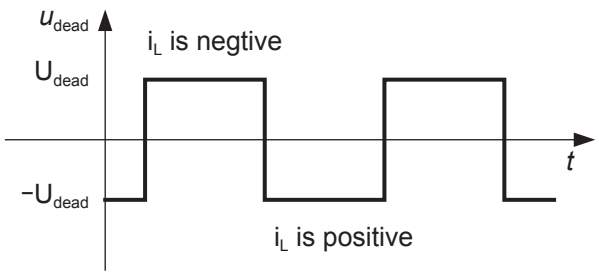

Fig. 4 Disturbance voltage equivalent to dead time effect.

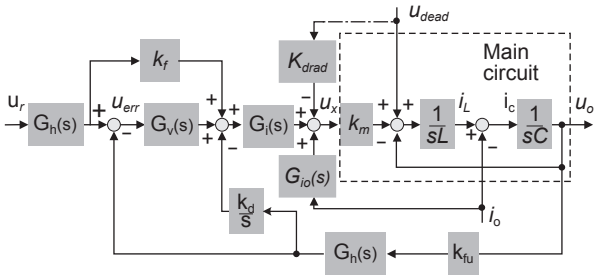

Fig. 5 Control diagram with dead time compensation and output current compensation.

It holds:

$$G_h(s) = \frac{1 - e^{-T_s s}}{s} \approx \frac{T_s}{0.5T_s s + 1} \tag{2}$$

where T_s is the sampling period.

After $G_h(s)$ is linearized, the standard design approaches such as Bode plot approach can be used to design the controllers $G_v(s)$ and $G_i(s)$. Then all the control parts should be discretized. In ref. 5 there is a comparison of several discretization methods for the application of switchmode power converters. The conclusion is that backward Euler method is the best one in terms of performance. Also backward Euler method is very simple, and s-domain function can be transferred to a z-domain by replacing "s" with "$\frac{1 - z^{-1}}{T_S}$". Thus, its method is chosen to all the control parts including dead time compensation and output current compensation as described below.

k_f is a feed-forward control element, which is conducive to decrease static error.

3.2 Dead time compensation

Referring to Fig. 1, specify that "1" denotes on-state and "0" denotes off-state. Then state (1, 0) denotes that VT_1 is on and VT_2 is off, and other situation is analogic. In each switching period there is two switches: one is (1,0) to (0,1), and the other is (0,1) to (1,0). Analyze the effect of dead time in two situations.

If i_L is positive:

As far as switch (1,0) to (0,1) is concerned, diode D_2 provides current immediately once VT_1 turns off, which is equivalent to on-state of VT_2. So dead time between switch (1,0) to (0,1) does not affect u_{in}.

As far as switch (0,1) to (1,0) is concerned, diode D_2 provides current until VT_1 turns on. So dead time between (0, 1) to (1, 0) prolongs negative time of u_{in}.

If i_L is negative:

To switch (0,1) to (1,0), diode D_1 provides current immediately once VT_2 turns off, which is equivalent to on-state of VT_1. So dead time between switch (0,1) to (1,0) does not affect u_{in}.

To switch (1,0) to (0,1), diode D_2 provides current until VT_1 turns on. So dead time between switch (1, 0) to (0, 1) prolongs positive time of u_{in}.

Combine the two situations and suppose i_L is an approximate sine wave with power frequency when load is heavy enough, dead time effect is equivalent to a square wave disturbance to u_{in} according to principle of area equivalence. The square wave is as shown in Fig. 4.

It holds:

$$U_{dead} = 2U_d T_d f_{switch} \tag{3}$$

where T_d is dead time, f_{switch} is switching frequency.

Feedforward compensation based on disturbance is available to weaken the dead time effect as shown in Fig. 5.

If $k_{dead} = 1/k_m$ holds, the effect on u_o of the distur-

bance u_{dead} will be eliminated.

Note that when an inverter feeds light load or no load, i_L can not be considered as a sine wave with power frequency, but a wave with switching frequency, then the dead time effect can be neglected. Then, the dead time compensation should be enabled only if the load is heavy. In this situation, inductor current i_L is similar to load current i_o. So it is reasonable to decide the sign of u_{dead} according to the sign of i_o in this paper.

A single phase UPS inverter is implemented using the proposed control scheme. Experimental results of the inverter under rated resistive load show that THD of u_o is 2.94% when the dead time compensation is disabled, while THD of u_o is 2.64% when its compensation is enabled. Thus, the proposed dead time compensation is effective.

4 Robust deadbeat control

In the circuit of a single-phase half-bridge UPS inverter (Fig. 1). If ESR of capacitor is neglected, the capacitor voltage u_c equals to the output voltage u_o. u_o and the inductance current i_L are chosen as state variables, and the load current i_o is treated as disturbance. The system state equation is

$$\dot{\boldsymbol{x}} = \boldsymbol{A} \cdot \boldsymbol{x} + \boldsymbol{B} \cdot u_{in} + \boldsymbol{D} \cdot i_o \tag{4}$$

$$y = \boldsymbol{C}^T \cdot x \tag{5}$$

where $x = [u_o\ i_L]^T$, $\boldsymbol{A} = [0\ 1/C\ ;\ -1/L\ 0]$, $\boldsymbol{B} = [0\ 1/L]^T$, $\boldsymbol{D} = [-1/C\ 0]^T$, $\boldsymbol{C} = [1\ 0]^T$

u_{in} is input voltage of LC filter (that is output voltage of inverter bridge) and is either $+U_d$ or $-U_d$ in the two level patterns.

The discrete state equation can be expressed as

$$x(k+1) = \boldsymbol{\Phi} x(k) + \mathbf{G}\,\Delta T(k) + \mathbf{P} i_o(k) + \mathbf{H} \tag{6}$$

where

$$\boldsymbol{\Phi} = e^{AT} = [\Psi_{11}\ \Psi_{12}\ ;\ \Psi_{21}\ \Psi_{22}]^T \tag{7}$$

$$\mathbf{G} = 2U_d e^{(AT/2)} \boldsymbol{B} = [g_1\ g_2]^T \tag{8}$$

$$\mathbf{P} = -\boldsymbol{A}^{-1}(I - e^{AT})\,\boldsymbol{D} = [p_1\ p_2]^T \tag{9}$$

$$\mathbf{H} = U_d A^{-1}(I - e^{AT})\,B = [h_1\ h_2]^T \tag{10}$$

where T is the control period, $\Delta T(k)$ is the acting time of positive voltage $+U_d$ in the kth control period.

In the traditional deadbeat control, the required pulse width $\Delta T(k)$ can be computed by making $u_o(k+1)$ in the first equation in 6 equal to the voltage reference $u_{ref}(k+1)$. It holds

$$\Delta T(k) = \frac{1}{g_1} u_{ref}(k+1) - \frac{\Psi_{11}}{g_1} u_o(k) - \frac{\Psi_{12}}{g_1} i_L(k) - \frac{P_1}{g_1} i_o(k) - \frac{h_1}{g_1} \tag{11}$$

Deadbeat control depends on the precise mathematical models of controlled object. Ideally the actual parameters of the inverter should be identical with calculating parameters used in equation11. However, the precise systemic model is difficult to be obtained; moreover, the actual parameters may change during operation.

A typical UPS inverter main circuit is considered to study the influence of parametric mismatching. Fig. 6 (a) shows the discrete system block diagram of traditional deadbeat control. Symbols with "^" stand for calculating values and symbols without "^" stand for actual values. The poor robustness makes it almost impracticable in UPS application. The proposed deadbeat control is shown in Fig. 6 (b). The difference between two types of control methods is a proportional element k_w added to the new proposal,

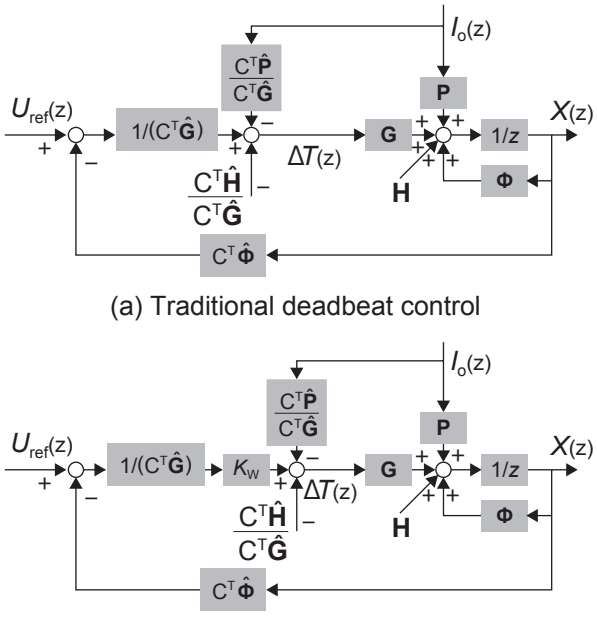

Fig. 6 Discrete system block diagram of deadbeat control for UPS inverter.

where usually $0 < k_w < 1$ and disappears if $k_w = 1$.

The transfer function from $U_{ref}(z)$ to $X(z)$ in Fig. 6 (b) is

$$\frac{X(z)}{U_{ref}(z)} = [\frac{C^T\hat{G}}{k_w}(zI - \Phi) + GC^T\hat{\Phi}]^{-1}G \quad (12)$$

The transfer function from voltage reference to output voltage is

$$G_i(z) = \frac{U_o(z)}{U_{ref}(z)} = \frac{C^T X(z)}{U_{ref}(z)} = C^T[\frac{C^T\hat{G}}{k_w}(zI-\Phi)+G\,C^T\hat{\Phi}]^{-1}G = \frac{k_w(g_1 z + g_2\Psi_{12} - g_1\Psi_2)}{q(z)} \quad (13)$$

where

$$q(z) = \hat{g}_1 z^2 + [g_1\hat{\Psi}_{11}k_w + g_2\hat{\Psi}_{12}k_w - \hat{g}_1\Psi_{22} - \hat{g}_1\Psi_{11}]z + g_2 k_w(\hat{\Psi}_{11}\Psi_{12} - \Psi_{11}\hat{\Psi}_{12}) + \Psi_{21}(g_1\hat{\Psi}_{12}k_w - \hat{g}_1\Psi_{12}) + \Psi_{22}(\hat{g}_1\Psi_{11} - g_1\hat{\Psi}_{11}k_w)$$

If $k_w = 1$, and the calculating values and the actual values are the same, equation 10 can be simplified as

$$G(z) = 1/z \quad (14)$$

It means that with the traditional deadbeat control, the output voltage follows the reference in one control period in case that there is no parametric mismatch.

Table 1 lists the constraints for actual parameters in traditional and proposed deadbeat control to make the system stable. It is obvious that constraints in the proposed method are much loose, and the control method is robust when actual parameters deviate from calculating parameters.

5 Experimental results

Experiments using the proposed robust deadbeat control method were carried out on a half-bridge inverter system.

Table 2 shows the static performance of the output voltage when the actual parameters of output filter deviate from the calculating parameters ($\hat{L}$ = 1.3 mH, $\hat{C}$ = 20 μF). L changes from 0.5 to 2.0 mH (38.5–153.8%$\hat{L}$), and C changes from 10 to 30 μF (50–150%$\hat{C}$). The prototype still has good performance when the deviation is within a certain range. The RMS value deviation of voltage is less than 2% under rated load and less than 4% under no load, and the THD of voltage is less than 1.5%. Only when both L and C are reduced to 38.5%$\hat{L}$ (0.5 mH) and 50% (30 μF), respectively, the system becomes unstable.

Table 3 shows performance comparison of the proposed robust deadbeat control and the digital PID control. The prototype has desirable static performance under different kinds of load. Besides, load change also causes little disturbance to the output voltage during dynamic process. Moreover, experimental results prove that the system can remain stable when actual parameters deviate from calculating parameters. Thus, with the proposed control method, the inverter has both small static error and

Table 1 Constraints for systemic parameters in deadbeat.

Parameters / Constraints	L / mH	C / μF	U_d / V
Traditional deadbeat	$\geq \hat{L}$	$\geq \hat{C}$	$\geq \hat{U}$ d
Proposed deadbeat (k_w = 0.7)	>70.23%$\hat{L}$	>49.1%$\hat{C}$	<146.94%$\hat{U}_d$

Table 2 Static performance with parametric deviation for proposed robust deadbeat control method.

Output filter		Rated load		No load	
L / mH	C / μF	U_o / V	THD / %	U_o / V	THD / %
2.0	30	100.3	1.09	101.5	1.07
1.5	30	100.0	1.11	102.1	1.07
1.0	30	100.5	1.12	102.4	1.07
0.5	30	100.9	1.19	102.9	1.20
2.0	20	100.3	1.10	102.3	1.05
1.5	20	100.5	1.10	101.4	1.11
1.0	20	100.6	1.13	101.8	1.13
0.5	20	101.0	1.30	103.3	1.34
2.0	10	100.1	1.12	101.5	1.14
1.5	10	101.2	1.15	101.9	1.17
1.0	10	101.4	1.27	103.1	1.30
0.5	10	Unstable			

Table 3 Performance comparison of the robust deadbeat control and the digital PID control.

	Proposed robust deadbeat control	Digital PID control
THD of output voltage under no load / %	1.57	2.51
THD of output voltage under rated load / %	1.56	2.64
THD of output voltage under rectifier load / %	2.82	3.8
Voltage regulation of output voltage / %	2.19	6.75
Sampling frequency / kHz	17.24	34.48

fast dynamic response and is robust for parametric deviation.

6 Conclusion

A novel digital control scheme for UPS inverter has been proposed. The quasi double loop control with dead-band compensation can make inverter working stable with small output filter. A novel deadbeat control method for UPS converters was also proposed to improve the performance of UPS inverters. A proportional element is added in this method to improve the robustness to systemic parameters. The method does not require much computation and can be easily realized in DSP. Systemic analysis and experimental results on this method prove that it greatly improves the robustness of deadbeat control and has good steady state performance.

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